

LISTING OF CLAIMS

1. (Currently Amended) A method of etching an integrated circuit (IC) structure having an ~~etched dielectric material~~ a first dielectric layer with an exposed a barrier layer, wherein said barrier layer is composed of a material consisting essentially of silicon nitride and is disposed below said first dielectric layer material, said barrier layer being disposed above a second layer having therein a metal interconnect co-planarly disposed adjacent to a dielectric material, said method comprising:

feeding a nitrous oxide (N_2O) gas and a fluoromethane (CH_3F) gas into a reactor;

generating a plasma in said reactor;

etching said barrier layer through a via that is disposed in said first dielectric layer,

wherein said etching said barrier layer etches down to said metal interconnect and partially etches said ~~etched dielectric material~~ with said plasma generated from said N_2O gas and said CH_3F gas; ~~and~~

~~generating a high selectivity between said barrier layer to said dielectric material.~~

2. (Original) The method of claim 1 wherein said dielectric material is comprised of materials that include silicon and oxygen.

3. (Currently Amended) The method of claim 2 wherein ~~said~~ a selectivity of said barrier layer to said dielectric material is 1.7 or more.

4. (Currently Amended) The method of claim 1 wherein said ~~etched~~ dielectric material is composed of a material selected from the group consisting of silicon dioxide, silicon oxide, organosilicate glass, SiLK, and fluorinated silicate glass.

5. (Original) The method of claim 1 further comprising depositing a thin barrier layer over said IC structure.

6. (Currently Amended) A method of etching an integrated circuit (IC) structure having ~~an~~ ~~etched a~~ first dielectric layer, a second barrier layer wherein said second barrier layer is composed of a material consisting essentially of silicon nitride, and a third layer having a copper interconnect co-planarly disposed adjacent to a dielectric material, said second barrier layer being disposed between said ~~etched~~ first dielectric layer and said third layer, comprising:

feeding a nitrous oxide (N_2O) gas and a fluoromethane (CH_3F) gas into a reactor;

generating a plasma in said reactor; and

etching said second barrier layer, wherein said etching said second barrier layer forms a via in said second barrier layer, said via at least partially overlaps said dielectric material thereby enabling said etching said second barrier layer to at least partially etches etch said first dielectric layer material with said plasma generated from said N_2O gas and said CH_3F gas; and terminating said etching said second barrier layer before said dielectric material is etched through.

~~generating a high selectivity between said barrier layer to said first dielectric layer; and~~

~~limiting oxidation of said third copper interconnect.~~

7. (Currently Amended) The method of claim 6 wherein ~~said a~~ selectivity of said ~~silicon~~
~~nitride~~ second barrier layer to said ~~etched~~ dielectric material is 1.7 or more.
8. (Currently Amended) The method of claim 6 wherein said ~~etched~~ first dielectric material
is composed of a material selected from the group consisting of silicon dioxide, silicon oxide,
organosilicate glass, SiLK, and fluorinated silicate glass.
9. (Original) The method of claim 6 further comprising depositing a thin barrier layer over
said IC structure.
10. (Currently Amended) A method of etching an integrated circuit (IC) structure having a
via etched into a first dielectric layer composed of a first dielectric material, a second barrier
layer wherein said second barrier layer is composed of a material consisting essentially of silicon
nitride, and a third layer having a conductive interconnect ~~surrounded by~~ co-planarly disposed
adjacent to a second dielectric material that comprises silicon and oxygen, said second barrier
layer being disposed between said ~~etched~~ first dielectric layer and said third layer, comprising:
feeding a nitrous oxide (N₂O) gas and a fluoromethane (CH₃F) gas into a reactor;
generating a plasma in said reactor;
etching said second barrier layer, wherein said etching said second barrier layer etches a
via through said second barrier layer to both said conductive interconnect and said second
dielectric material, whereby said etching said second barrier layer partially etches said first
second dielectric material with said plasma generated from said N₂O gas and said CH₃F gas and
terminates before said second dielectric material is etched through;

~~generating a high selectivity between said barrier layer to said first dielectric material and
said second dielectric material; and
limiting oxidation of said third copper interconnect.~~

11. (Currently Amended) The method of claim 10 wherein ~~said~~ a selectivity of said ~~silicon nitride~~ second barrier layer to said ~~etched~~ second dielectric material is 1.7 or more.

12. (Currently Amended) The method of claim 11 wherein said ~~first~~ second dielectric material is composed of a material selected from the group consisting of silicon dioxide, silicon oxide, organosilicate glass, SiLK, and fluorinated silicate glass.

13. (Original) The method of claim 12 further comprising depositing a thin barrier layer over said IC structure.

14. (Currently Amended) The method of claim 10 wherein said via and said conductive interconnect are misaligned, thereby causing said via to extend to both said conductive interconnect and said second dielectric material., ~~and during said etching of said silicon nitride barrier layer, said second dielectric material is partially etched and a cavity is formed in said second dielectric material.~~

15. (Currently Amended) The method of claim 14 further comprising depositing a thin barrier layer over said IC structure that covers said cavity and said via, ~~said via and said trench.~~